IN THE SPECIFICATION:

Please amend the specification as follows:

Paragraph beginning on page 1, at prenumbered line 21, has been amended as follows:

In order to improve the electrical performance of a semiconductor package, the substrate includes at least one ground/power layer between the contact pads and the ground/power ring. A substrate using a multi-layer PWB is disclosed in R.O.C. Patent No. 434664 entitled "lead-bond type chip package and manufacturing method thereof". The substrate includes an interlayer circuit board having ~~prepeg~~ pre-preg disposed thereon. The interlayer circuit board possesses a metal ground/power plane so as to connect the ground/power source. Nevertheless, when a plurality of through holes are massively formed on multi-layer substrate for electrically connecting with lead fingers (signal), the through holes can not electrically be connected with the ground/power plane by forming a plurality of openings in the ground/power plane. Therefore, each opening is round corresponding to each through hole in position, enables the through holes to electrically insulate against the ground/power plane. However, electrical performance of the package substrate will be imparied when the through holes in the ground/power plane are mass and in irregular distribution.

Paragraph beginning on page 3, at prenumbered line 17, has been amended as follows:

As ~~showed~~ shown in Fig. 1, according to the present invention a package substrate 100 for improving electrical performance mainly comprises a first insulating layer 110, a wiring layer and at least a ground/power layer (which includes a ground layer 140 and a power layer 150). The first insulating layer 110 is made of glass fiber reinforced resin of FR-4, FR-5, BT resin, or a soft insulating layer, such as polyimide. The first insulating layer 110 has a top surface 111 and a bottom surface 112. The top surface 111 includes a chip-attaching region 113 for attaching a semiconductor chip 200 (referring to Fig. 1 and 4). The wiring layer is formed on top surface 111 of the first insulating layer 110. As ~~showed~~ shown in Fig. 1 and Fig. 2,

the wiring layer includes a plurality of inner fingers 121, a plurality of outer fingers 131 and a plurality of traces 122, 132. The inner fingers 121 and the outer fingers 131 are distinguished according to the distances from the chip-attaching region 113. The inner fingers 121 are closer to the chip-attaching region 113 than the outer fingers 131. Both the inner fingers 121 and outer fingers 131 are used to electrically connect the signals of a semiconductor chip 200. Also, a plurality of inner through holes 123 are electrically connected with the inner fingers 121 by corresponding traces 122. A plurality of outer through holes 133 are electrically connected with the outer fingers 131 by corresponding traces 132. The inner through holes 123 and the outer through holes 133 are formed through the first insulating layer 110 to electrically connect the top surface 111 and the bottom surface 112. In this embodiment, the wiring layer further includes a ground metal ring 160 and a power metal ring 170 around the chip-attaching region 113. The inner fingers 121 are disposed between the metal ring 160, 170 and the outer fingers 131.

Paragraph beginning on page 4, at prenumbered line 12, has been amended as follows:

In this embodiment as ~~showed~~ shown in Fig. 1 and Fig. 3, the ground layer 140 is formed on the bottom surface 112 of the first insulating layer 110 as a ground for the chip 200, which may be a copper foil or other metal foil. The package substrate 100 can further includes a second insulating layer 180 disposed on the bottom surface 112 of the first insulating layer 110 to sandwich the ground layer 140 between the first insulating layer 110 and the second insulating layer 180. At least a ground through hole 161 is formed through the first insulating layer 110 so as to connect the ground metal ring 160 and the ground layer 140 at different planes. The ground layer 140 has a plurality of openings 141. The openings 141 are arranged radially to the chip-attaching region 113 in a shape of strip or circle, wherein the openings 141 in a strip-shaped are formed for passing through a mass of inner through holes 123 crowded in groups. Thus the inner through holes 123 are divided into a plurality of groups. Each group of the inner through holes 123 arranges in single-line or multi-line grid array and is formed through each corresponding opening 141, but electrical isolated from the ground layer 140. Therefore the ground layer

140 has a strip-shaped region between two adjacent openings 141. The strip-shaped region of the ground layer 140 between two adjacent openings 141 is not less than 0.2mm in width to provide a satisfied current path 142.